CLAIMS

What is claimed is:

1. A device comprising:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a plane metallization layer within the device;

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer, and electrically isolated from the plurality of component mounting pads.

2. The device of claim 1 wherein the plane metallization layer is a power plane.

3. The device of claim 1 wherein the plane metallization layer is a ground plane.

4. The device of claim 1 wherein the plane metallization layer is a reference voltage plane.

5. The device of claim 1 further comprising a signal carrying plated through hole which passes though the plane metallization layer within the device and terminates at a component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads.

6. The device of claim 5 wherein the signal carrying plated through hole which passes though the plane metallization layer is electrically isolated from the plane metallization layer and is connected to a component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads.

7. The device of claim 1 wherein the device forms a printed circuit board.

8. The device of claim 1 wherein the device forms a semiconductor chip.

9. The device of claim 1 wherein the plated through hole is a via.

10. A system comprising:

a processor;

a memory communicatively coupled to the processor; and

a device associated with at least one of the memory or the processor further including:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a plane metallization layer within the device; and

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads.

11. The system of claim 10 wherein the device is a printed circuit board.

12. The system of claim 10 wherein the device is a portion of a semiconductor chip.

13. The system of claim 10 wherein the plane metallization layer is a ground plane.

14. The system of claim 10 wherein the plane metallization layer is a power plane.

15. The system of claim 10 wherein the plane metallization layer is a reference voltage plane.

16. The system of claim 10 wherein the signal carrying plated through hole which passes though the plane metallization layer is electrically isolated from the plane metallization layer and is connected to a component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads.

17. A device comprising:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a first plane metallization layer within the device;

a second plane metallization layer within the device;

a first plane plated through hole attached to at least one of the first plane metallization layer and the second plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the first plated through hole attached to the plane metallization layer electrically isolated from the plurality of component mounting pads.

18. The device of claim 17 further comprising a signal carrying plated through hole which passes though the first plane metallization layer and is electrically isolated from the first plane metallization layer, the signal carrying plated through hole passes through the second plane metallization layer and is electrically isolated from the second plane metallization layer, the signal carrying through hole connected to a component mounting pad at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads.

19. The device of claim 18 wherein the first plane plated through hole is attached to both the first plane metallization layer and the second plane metallization layer.

20. The device of claim 18 wherein the first plane plated through hole is attached to the first plane metallization layer, the device further comprising a second plane plated through hole attached to the second plane metallization layer, the second plated through hole terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the second plated through hole attached to the second plane metallization layer electrically isolated from the plurality of component mounting pads.

21. A method for testing a device having a signal carrying through hole that passes though an internal plane within the device, and has a pad for connecting to the signal carrying through hole on the exterior surface of the device, the method comprising:

terminating a plane through hole connected to an internal plane at the exterior surface of the device;

contacting the signal carrying through hole;

contacting the plane through hole; and

checking for current flow between the signal carrying through hole and the plane through hole.

22. The method of claim 21 further comprising failing the device if current flows between the signal carrying through hole and the plane through hole.

23. The method of claim 21 further comprising passing the device if current does not flow between the signal carrying through hole and the plane through hole.

24. The method of claim 23 further comprising adding electrical components to the device.

25. The method of claim 21 wherein contacting the signal carrying through hole, and contacting the plane through hole is done from the same side of the device.

26. The method of claim 21 wherein contacting the signal carrying through hole, and contacting the plane through hole is done substantially simultaneously.

27. The method of claim 21 wherein checking for current flow between the signal carrying through hole and the plane through hole is done before connecting the device to other devices.

28. A device comprising:

a first major exterior surface;

a second major exterior surface, at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads;

a feature positioned within the device;

a plated through hole attached to the plane metallization layer and terminating at the at least one of the first major exterior surface and the second major exterior surface including a plurality of component mounting pads, the plated through hole attached to the feature within the device, and electrically isolated from the plurality of component mounting pads.

29. The device of claim 1 wherein the feature is an electrical trace.

30. The device of claim 1 wherein the feature is a plane metallization layer.